Closed–Loop, Needless PID Controller Based on the Difference Between Measured and Calculated Arm Voltages for MMC

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Abstract— Power conversion from ultra-voltage DC (UVDC) to ultra-voltage AC is the greatest challenge facing industrial power application companies, such as ABB and Siemens. Converting UVDC transmission systems, which are used to transmit power long distances of up to 3,000 Km and ultra-voltages up to 2,200 KVDC, to UVAC is the most challenging issue associated with transmitting power with a UVDC transmission system. This paper proposes a closed-loop, needless PID controller for a modular multilevel converter (MMC) with a large scale of submodules per arm to convert UVDC 2,200 KV and more to UVAC, in order to achieve total harmonics distortion (THD) for UVAC of less than 1%. First, insertion indices are generated by utilizing the difference in arm voltage between the measured voltage and calculated voltage of each arm, which is considered the starting point for the proposed algorithm, from which to derive the number of submodules per arm (N). Secondly, flooring switching pulse-width modulation (PWM) is explained in order to generate the number of inserted and bypassed submodules per arm. Thirdly is an analysis of the balancing between the submodules' voltages and submodule selection, which is the key technique for a modular multilevel converter with UVDC application that is proposed and verified by simulations. Fourthly, a set of simulation results is presented for the 2,200-KV DC bus and the 481-level for the output voltage, in order to verify the proposed algorithm; the simulation was conducted in a MATLAB/Simulink environment. Finally, the proposed algorithm was verified experimentally through the prototype's hardware and software designs. The experimental results are also documented in this paper.

Index Terms— Closed loop control for MMC.

1 Introduction

MMC had been invented by Lesnicar and Marquardt as a development from the Cascaded H-Bridge Converter [1]. MMC was first presented as AC to AC and DC to AC converters, for high-power experimental prototypes [6]. MMC was presented as a cascaded converter based on cascading identical submodules [7]. The selection submodules have to be inserted or bypassed for each arm of the converter while maintaining each submodule capacitor voltage around its reference voltage, and phase arm modulation is an important aspect of the operation of the converter. The submodule, the heart of an MMC, has had its operation and circuit configuration explained before [1], [12], [13]. [12] simplifies the MMC by considering the sum of capacitors voltages in each arm instead of individual capacitor voltage. A number of papers discussed modulation methods based on multilevel SPWM for MMC topology in the technical literature [13], [15]. The modeling of nonlinear control of MMC was introduced in [19]. PWM for a limited number of voltage levels was presented in [21], which used average PWM pattern over a switching period to determine switching of MMC. [23] described the number of connected or bypassed submodules by direct modulation for a small number of submodule per arm based on the floor value between the reference sinusoidal signal and the number of submodules for each arm. Optimizing MMC patterns has also been a subject of research, with [24] studying MMC under selective harmonic elimination PWM and a fundamental frequency switching pattern as in [25]. Different control approaches with various modulations were presented in [25] and [26] to investigate dynamic and required voltage balance of MMC topology. A number of applications such as voltage source converter-based HVDC transmission and back-to-back converter had been studied based on the use of MMC [21] and [27]. Also, in [28] and [29], high-voltage super-grids provided the possibility of using MMC in the configuration for multi-terminal HVDC. The modular topologies classification, presented in [7], does not rate the converter as a topology with many useful submodules for a DC system that can transmit up to 2200 KV. Power losses for both the converter and its submodules were evaluated in [30] and in [31], submodules losses were evaluated by utilizing different configurations for MMC. The effect of sampling frequency on THD in the operation of the converter was analyzed in [32]. Also, the effect of dead time in the submodule of the converter was considered in [33]. [34] presented minimization method of DC-link ripple, a mathematical model for the capacitor voltage variations, and improved voltage balancing control system for MMC in the converter topology [35]. Arm inductance and submodule capacitance can be calculated in different methods as in [37], [38], and [39]. Also, a smoothing reactor for HVDC systems has been evaluated exactly [40] and approximated [41]. Transmitting power 10,000 MW and distance up to 3000 km with ± 1100 kV DC is considered economic, efficient, mature technology [6] and [42]. The DC bus voltage of UHVDC transmission system determines the number of submodules per arm. Therefore, with 2200 KVDC ([6], [42], [43]), each converter arm consists of a large number of submodules. Our literature review suggests a topology for MMC and proposed PWM algorithm is needed to fulfill the requirements of UHVDC bus voltage in this paper with the following contributions:

a. For UHVDC Systems

- There will be demand for UHVDC in the next year (2200 KV and more) The paper proposes MMC topology with more submodules per arm to achieve the large scale of output voltage levels based on simple algorithm control.
- Since the number of submodules is hundreds in UHVDC, sinusoidal AC voltage waveforms will be achieved and THD will be limited to less than one to avoid using AC filters.
- The proposed method works with low switching frequency for UHVDC systems, which will decrease converter losses.

b. For MMC itself

- The proposed method offers a simple numerical algorithm for MMC topology that can be used with a large or small number of submodules per arm either experimentally or by simulation.
- The selection process for inserting or bypassing submodules guarantees capacitors voltages around the reference voltage (Vdc/N) with voltage ripple less than 7% even for a large number of submodules per arm.
- More converter stability can be achieved by equal sharing of currents from both arms to the load.

2 Operation Principles and Converter Equations

Figure 1 illustrates a final single-phase MMC circuit. Since the capacitors are not guaranteed to provide constant voltage when connected to a circuit, this brings some problems. If a capacitor is inserted in the arm, its voltage varies according to the direction of the current. The simplest and accurate solution is to use the effect that charges and discharges the capacitors actively in the converter modulation itself through a specific algorithm to be explained in detail later in this paper. However, capacitor voltages are still inconstant, something which could cause current transience due to unequal voltages between the legs. For this reason, inductances are also placed in each arm. The heart of the MMC is the submodule. It's basic half-bridge scheme appears in Figure 2. Each submodule contains a DC storage capacitor C, a half-bridge composed of two switching elements T1 and T2 with the freewheeling diodes D1 and D2. When the current flows from the DC side in the direction of the AC terminals, its route follows the green line. When it flows in the opposite direction, its route follows the red line.

If both switches are OFF, the current charges the capacitor through the freewheeling diode D1, in the green flow. In the red flow, the current passes through the diode D2, bypassing the capacitor. If T1 is switched ON, the voltage of the capacitor is applied across the terminals of the submodule. In the green flow, the current charges the capacitor through D1; in the red flow, it discharges the capacitor through T1. When T2 is switched ON, the terminals of the submodule are short-circuited and the current flows through T2 or D2, depending on the direction of the current. In the latter situation and based on the proposed algorithm, the capacitor maintains its state of charge and its voltage remains unchanged. Using these switching states, it is possible to control each of the submodules separately. Table I shows switching states for the submodule.

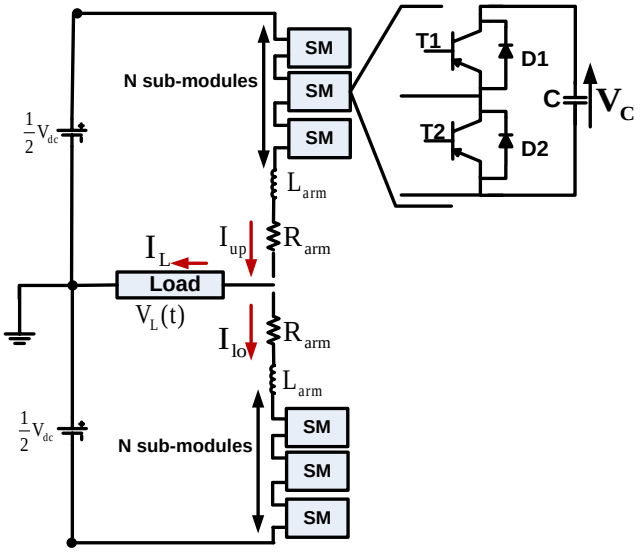

Figure 1. Single-phase MMC circuit.

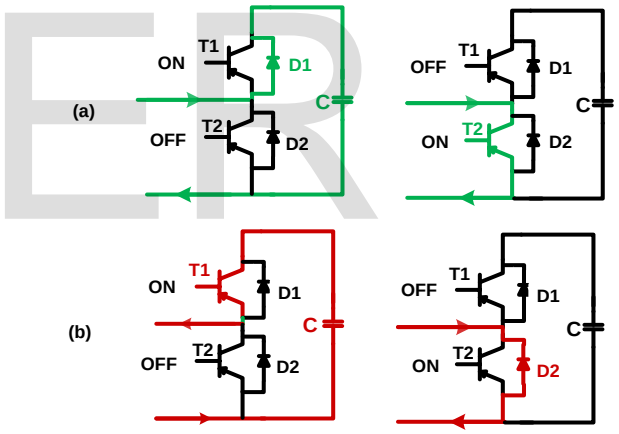

Figure 2. (a) Positive and (b) negative current flow inside an MMC submodule.

TABLE I
SWITCHING STATES FOR EACH SUBMODULE

T1	T2	D1	D2	Current direction	Capacitor state	Output voltage
OFF	ON	OFF	OFF	Iarm>0	Uncharged (bypassed)	0
OFF	OFF	OFF	ON	Iarm<0	Uncharged (bypassed)	0
OFF	OFF	ON	OFF	Iarm>0	Charging	VC
ON	OFF	OFF	OFF	Iarm<0	Discharging	VC

To explain how the proposed PWM algorithm works for MMC circuit, a specific example will show how to generate a voltage waveform. In this example, the number of submodules

per each leg will be 5; the converter will convert DC to AC with the 6-level waveform (n=N+1; where n number of output voltage level), which will be explained in detail. The voltage across each capacitor can be given as in (1):

$$V_C = \frac{V_{dc}}{N} = \frac{V_{dc}}{4}\ V. \qquad (1)$$

V_{dc} is DC bus voltage, and assuming the submodule selection process is effective, the submodule capacitors within a converter arm can be assumed to be equally charged. This is possible with a switching frequency high enough to allow the modulator to act even on very small disturbances in this balance. It will be proven later that these assumptions can apply for a small number of submodules. Figure 1 shows an equivalent electrical circuit for one phase leg of MMC and Table 2 shows MMC parameters definitions.

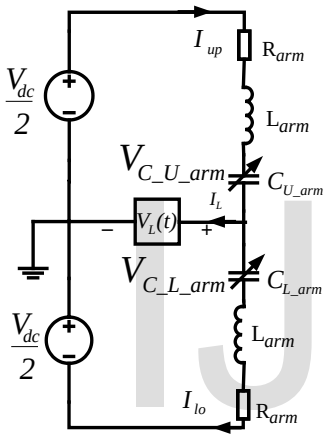

Figure 3. Equivalent electrical circuit for one phase leg of MMC.

TABLE II
MMC PARAMETER DEFINITIONS

C	Submodule capacitance
x	Insertion index
I_{up}	Upper arm current
I_{lo}	Lower arm current
Icir	Circulating current
I_{out}	Output phase current
xU	Insertion indices of the upper arm
xL	Insertion indices of the lower arm
$V_{C\ U\ arm}(t)$	Total upper arm capacitor
$V_{C\ L\ arm}(t)$	Total lower arm capacitor
V_{dc}	DC bus
V_{out}	Output phase voltage

$$C_{arm} = \frac{C}{N\,.\,x}. \qquad (2)$$

Let the converter consist of N submodules per arm. In general, each arm is controlled by an insertion index x, which is defined such that x = 0 means that all N submodules in the arm are bypassed, while x = 1 means that all N submodules in the arm are inserted. In the former case, the current is flowing through the arm will not pass through any capacitor, so the equivalent capacitive arm impedance is zero. In the latter case, the arm current will meet N capacitors connected in series, making the equivalent capacitance of the arm C/N. If each submodule capacitor has capacitance C, the effective capacitance of the one arm is given by (2):

Let the total voltage stored in the capacitors of each arm be Vc(t). Then the voltage inserted by the arm is given by (3).

$$V_{C\_arm}(t) = x\,.V_C(t). \qquad (3)$$

The total capacitor voltage will be increased when a charging current passes through the arm as in (4).

$$\frac{dV_C(t)}{dt} = \frac{N}{C}\,.x\,.\,I_{arm}(t). \qquad (4)$$

Naming the upper and lower arm currents I_{up} and I_{lo} respectively, and defining their polarities as illustrated in Figure 1, the output phase current is calculated as their sum in (5).

$$I_{out} = I_{up} - I_{lo}. \qquad (5)$$

The output phase current is assumed to be equally shared by both upper and lower arm. However, and as mentioned in previous paragraphs, there is a deviation from this ideal condition since part of the current passes through the series-connected arms and the DC source. Let this circulating current be called I_{cir} as in (6).

$$\left.\begin{aligned} I_{up} &= I_{cir} + \frac{I_{out}}{2} \\ I_{lo} &= I_{cir} - \frac{I_{out}}{2} \end{aligned}\right\} \xrightarrow{\sum} I_{cir} = \frac{I_{up} + I_{lo}}{2}. \qquad (4)$$

In a three-phase system, $I_{cir}=(1/3)I_{dc}$ and in a single phase system, $I_{cir}=I_{dc}$.

Defining xU and xL as the insertion indices of the upper and the lower arm respectively, the following equations (7) and (8) are derived:

$$\frac{dV_{C\_U\_arm}(t)}{dt} = \frac{N}{C}\,x_U\,I_{up} = \frac{1}{C_{arm}}\,x_U\,I_{up} \qquad (7)$$

$$\frac{dV_{C\_L\_arm}(t)}{dt} = \frac{N}{C}\,x_L\,I_{lo} = \frac{1}{C_{arm}}\,x_L\,I_{lo} \qquad (8)$$

$V_{C\_U\_arm}(t)$ and $V_{C\_L\_arm}(t)$ are total upper arm capacitor and total lower arm capacitor respectively.

Finally, from the model analysis of the circuit in Figure 3,

and by taking into account resistance R_{arm} and inductance L_{arm} of each arm, it is found that:

$$\frac{V_{dc}}{2} - R_{arm} I_{up} - L_{arm} \frac{dI_{up}}{dt} - x_U V_{C\_U\_arm} = V_{out} \quad (9)$$

$$-\frac{V_{dc}}{2} - R_{arm} I_{lo} - L_{arm} \frac{dI_{lo}}{dt} - x_L V_{C\_L\_arm} = V_{out} \quad (10)$$

Where V_{out} the output phase voltage, by solving the last two equations, the equivalent voltage for the external load connected to the AC terminal becomes:

$$V_{out} = \frac{x_L V_{C\_L\_arm} - x_U V_{C\_U\_arm}}{2} - \frac{R_{arm}}{2} I_L - \frac{L_{arm}}{2} \frac{dI_L}{dt} \quad (11)$$

It is obvious from (6) that upper arm current generates the positive half cycle for the output AC current while lower arm current generates its negative half cycle. Also, from (11), it is obvious that upper arm voltage generates the negative half cycle of output AC voltage while lower arm voltage generates its positive half cycle of the output AC voltage as will be proved by computer simulation and experimental prototype.

3 Proposed PWM Algorithm

Figure 4 shows the general flowchart for the proposed PWM algorithm.

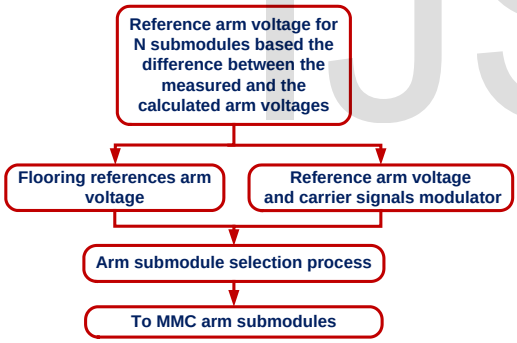

Figure 4: Proposed PWM algorithm flowchart

These steps will be discussed in details, in order to provide a deep understanding of the PWM algorithm's generation for N submodules, as follows:

3.1 Reference the arm voltage for N submodules based on the difference in arm voltage between the measured and calculated voltage

The proposed PWM algorithm for MMC is based on the equalization of the inserted submodules for one arm with the bypassed submodules of the other arm. First, the operation of MMC as a (N+1) level converter is discussed. The principle is that, at each instant, N submodules are inserted and N modules are bypassed for the whole leg. Let N_U be the number of submodules inserted into the upper arm and N_L be the number of submodules inserted into the lower arm. Accordingly, the AC terminal can take N + 1 different potentials when the number of inserted modules varies between 0 and N. Since the equation for stored energy in a capacitor is $W=(1/2)*CV^2$, the upper and lower arms' energy equations can be written as follows:

$$W_{C\_U\_arm}(t) = \frac{1}{2} * C_{U\_arm} * \left(V_{C\_U\_arm}(t)\right)^2 \quad (12)$$

$$W_{C\_L\_arm}(t) = \frac{1}{2} * C_{L_{arm}} * \left(V_{C_{\_L\_arm}}(t)\right)^2. \quad (13)$$

$\frac{V_{C\_L\_arm} - V_{C\_U\_arm}}{2}$, part of (11), is considered the main part of the output voltage and can be given as variable E_L, as in (14).

$$E_L = \frac{V_{C\_L\_arm} - V_{C\_U\_arm}}{2}. \quad (14)$$

From the voltage loops in Figure 3, arm impedance is small compared to the capacitors' voltage; thus, (15) can be given as follows:

$$V_{dc} \approx \left(V_{C_{U_{arm}}} + V_{C_{L_{arm}}}\right). \quad (15)$$

Both equations in time, for E_L and load current I_L,, can be written as (16) and (17):

$$E_L(t) = \hat{E}_L \cos(\omega t) \quad (16)$$ $\hat{E}_L$

$$I_L(t) = \hat{I}_L \cos(\omega t + \emptyset), \quad (17)$$

where $\hat{E}_L$ is the maximum output voltage and $\hat{I}_L$ is the maximum output current. The main target of the arms' energy approximation control is to calculate the modulation indices of x_U and x_L, for both the upper and lower arms, respectively. Since the circulating current is DC, it will not cause an inductive voltage drop. Therefore, $\left(L_{arm} * \frac{dI_{cir}}{dt}\right)$ can be neglected. Further, it is assumed that the circulating current only has a DC component (i.e., there is no AC component):

$$I_{cir} = I_{cir\_DC}. \quad (18)$$

Arm voltage can be measured by measuring the voltage across each capacitor submodule for both arms:

$$V_{C\_U\_arm}^{Mea.} = \sum_{i=1}^{i=N} V_{c\_U\_i}^{Mea.} \quad (19)$$

$$V_{C\_L\_arm}^{Mea.} = \sum_{i=1}^{i=N} V_{c\_L\_i}^{Mea.}. \quad (20)$$

The reference voltage for both arms can be calculated as follows:

$$V_{C\_U\_arm}^{Cal.} = N * \left(\frac{V_{dc}}{N}\right) = V_{dc} \quad (21)$$

$$V_{C\_L\_arm}^{Cal.} = N * \left(\frac{V_{dc}}{N}\right) = V_{dc}. \quad (22)$$

From (19) and (21) together, as well as from (20) and (22), the change in arm voltage between the measured and calculated voltage can be written as follows:

$$\Delta V_{C\_U\_arm} = V_{C\_U\_arm}^{Mea.} - V_{C\_U\_arm}^{Cal.} \quad (23)$$

$$\Delta V_{C\_L\_arm} = V_{C\_L\_arm}^{Mea.} - V_{C\_L\_arm}^{Cal.}. \quad (24)$$

Using (23) and (24), the reference voltages for both the upper and lower arms can be calculated as follows:

$$V_{C\_U\_arm}^{ref} = \frac{V_{dc}}{2} - \hat{E}_L \cos(\omega t) - \Delta V_{C\_U\_arm} \quad (25)$$

$$V_{C\_L\_arm}^{ref} = \frac{V_{dc}}{2} + \hat{E}_L \cos(\omega t) - \Delta V_{C\_L\_arm}. \quad (26)$$

As mentioned before, since the circulating current is DC, it will not cause an inductive voltage drop. Furthermore, the drop in voltage across the resistance is very small and can be neglected. Also, by referring to the output voltage in (5) and (8), the output voltage equation can be rewritten as follows:

$$\hat{V}_L \cos(\omega t) = \frac{V_{dc}}{2} \cos(\omega t) = E_L(t) = \hat{E}_L \cos(\omega t). \quad (27)$$

By using assumption (27), both (25) and (26) can be rewritten as follows:

$$V_{C\_U\_arm}^{ref} = \frac{V_{dc}}{2} - \frac{V_{dc}}{2} \cos(\omega t) - \Delta V_{C\_U\_arm} \quad (28)$$

$$V_{C\_L\_arm}^{ref} = \frac{V_{dc}}{2} + \frac{V_{dc}}{2} \cos(\omega t) - \Delta V_{C\_L\_arm}. \quad (29)$$

By using the differentiation of arms energies equations, the differentiation of leg energy equation can be written as follows:

$$\frac{dW_{leg}}{dt} = (V_{dc} - 2 * R_{arm} I_{cir\_DC}) * I_{cir\_DC} - \frac{\hat{V}_L * \hat{I}_L}{2} * [\cos(\emptyset) + \cos(2\omega t + \emptyset)]. \quad (30)$$

Since $\hat{V}_L = \frac{V_{dc}}{2}$ and $\hat{I}_L = \frac{\hat{V}_L}{|Z_{load}|} = \frac{V_{dc}}{2*|Z_{load}|}$, (19) can therefore be rewritten as follows:

$$\frac{dW_{arm}}{dt} = (V_{dc} - 2 * R_{arm} I_{cir\_DC}) * I_{Diff\_DC} - \frac{{V_{dc}}^2}{8 * |Z_{load}|} * [\cos(\emptyset) + \cos(2\omega t + \emptyset)]. \quad (31)$$

Since the offset component of the energy derivative must disappear in order to achieve the steady-state condition, (31) will equal zero in order to get the DC circulating current I_{Diff_DC} for this condition, as given by (32).

$$I_{cir\_DC} = \frac{V_{dc}}{2} * \left(1 - \sqrt{1 - \frac{R_{arm}}{|Z_{load}|} \cos(\emptyset)}\right). \quad (32)$$

The individual arm energies W_{C_Uarm} and $W_{C\_L\_arm}$ can be obtained by solving the differentiation of arm energy equations, while taking into account the assumption in (27) and the given values $\hat{V}_L = \frac{V_{dc}}{2}$ and $\hat{I}_L = \frac{\hat{V}_L}{|Z_{load}|} = \frac{V_{dc}}{2*|Z_{load}|}$. The results are described by (33) and (34):

$$W_{C\_U\_arm} = W_{C\_U\_0} - \frac{1}{Z_{load}} * \left(\frac{(V_{dc})^2 * sin(\omega t + \emptyset) - 2 * R_{arm} * I_{cir_{DC}} * V_{dc}}{(8 * \omega)} + \frac{(V_{dc})^2 * sin(2\omega t + \emptyset)}{(32 * \omega)}\right) - \frac{(I_{cir\_DC} * V_{dc} * sin(\omega t))}{(2 * \omega)} \quad (33)$$

$$W_{C\_L\_arm} = W_{C\_L\_0} + \frac{1}{Z_{load}} * \left(\frac{(V_{dc})^2 * sin(\omega t + \emptyset) - 2 * R_{arm} * I_{cir\_DC} * V_{dc}}{(8 * \omega)} + \frac{(V_{dc})^2 * sin(2\omega t + \emptyset)}{(32 * \omega)}\right) - \frac{(I_{cir\_DC} * V_{dc} * sin(\omega t))}{(2 * \omega)}, \quad (34)$$

where $V_{C\_U\_0}$ and $V_{C\_L\_0}$ are the integration constants. Initially, as far as the energy references of the controllers are concerned, they were chosen to fulfill the typical steady state operation conditions of an MMC. For this reason, the energy references are set as in (12), which apparently corresponds to the total arm capacitor voltage.

$$W_{C\_0} = W_{C\_U\_0} = W_{C\_L\_0} = \frac{1}{2} * C_{arm} * (V_{dc})^2 \ J. \quad (35)$$

The total arm capacitor voltages $V_{C\_U\_arm}$ and $V_{C\_L\_arm}$ can be calculated as given in (36) and (37). The modulation of the modular multilevel converter is based on the equalization of the inserted submodules for one arm with the bypassed submodules for the other arm.

$$V_{C\_U\_arm}(t) = \left(\frac{2 * W_{C\_U\_arm}(t)}{C_{U\_arm}}\right)^{\frac{1}{2}} \quad (36)$$

$$V_{C\_L\_arm}(t) = \left(\frac{2 * W_{C\_L\_arm}(t)}{C_{L\_arm}}\right)^{\frac{1}{2}}. \quad (37)$$

The principle is that N modules are inserted and N modules are bypassed at each instant. Let n_U be the number of modules inserted into the upper arm and n_L be the number of modules inserted into the lower arm. Accordingly, the AC terminal can take N + 1 different potentials when the number of inserted modules varies between 0 and N. The modulator can now be fed by the modulation indices that can be computed from (39) for the upper arm and (40) for the lower arm. The main target

of this process is to get the number of inserted submodules for both arms while keeping the condition of this method, as given in (38).

$$\left.\begin{aligned} N_{U,bypassed} &= N - N_{L,bypassed} = N_{L,inserted} \\ N_{U,inserted} &= N - N_{L,inserted} = N_{L,bypassed} \end{aligned}\right\} \longrightarrow \quad (38)$$

$$x_U = \frac{V_{C\_U\_arm}^{ref}}{V_{C\_U\_arm}} \times N \qquad 0 < x_U \leq N \qquad (39)$$

$$x_L = \frac{V_{C\_L\_arm}^{ref}}{V_{C\_L\_arm}} \times N \qquad 0 < x_L \leq N. \qquad (40)$$

This step is considered to be the starting point for arm energy approximation control PWM, as can be seen later. Figure 5 shows the number of inserted submodules for both the upper and lower arms as described in (39) and (40), in sinusoidal waveform.

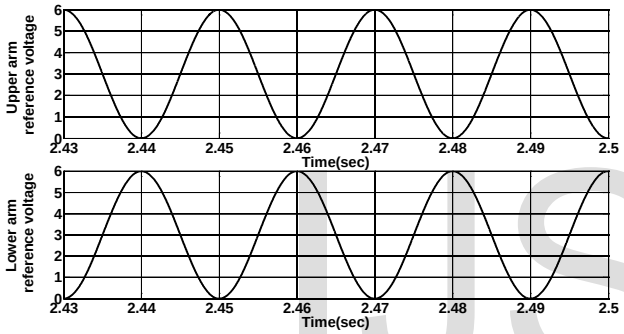

Figure 5. Reference voltage and number of inserted submodules for both arms.

3.2 Flooring arms voltages references

Since the numbers of inserted or bypassed submodules for both arms are real, positive and integer numbers, flooring the sine waves of both the upper and lower arms must be done for this purpose. Floor value (a) requires choosing the value of (a) to the nearest integer in the direction of negative infinity, while ceiling value (a) involves choosing (a) to the nearest integer in the direction of positive infinity. For example, the floor value for 0.5 is 0, and the floor value for 1.99 is 1. Figure 6 shows both numbers of inserted submodules for both arms after flooring (the red signal is N before flooring, while the blue signal is N after flooring).

3.3 References arms voltages and carrier signals modulator

At the same time as the last step, the modulation process is conducted on the reference signals of both the upper and lower arms with the carrier signal that has a switching frequency for the switches, as can be seen in Figure 7. The modulator will modulate both signals to the waveform in Figure 8 for both the upper and lower arms, respectively, in a process that creates a signal to match an assigned reference, by averaging the number of inserted submodules between a floor and a ceiling number in every sampling period. This process determines the inserted submodules for both the upper and lower arms and the exact instants of the switching actions. Figure 8 shows the inserted submodules for both the upper and lower arms at the same time. It is obvious that the number of inserted submodules in one arm is equal to the number of bypassed submodules ($N - N_{L\_inserted}$) in the other arm, which balances the voltages between the upper and lower arms across the AC terminal. As described in the previous paragraphs, the MMC output and circulating currents are determined by the state of the submodules within the converter's arms. The voltage determining the converter's output current is derived by the variation of the submodules' voltages connected to the upper and lower arms.

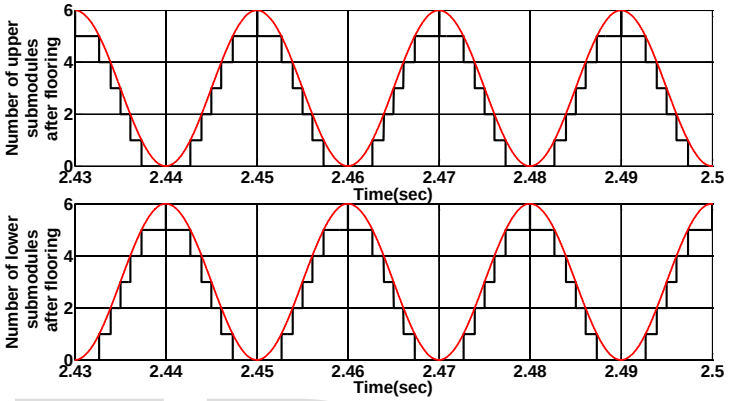

Figure 6. Number of upper and lower submodules after flooring.

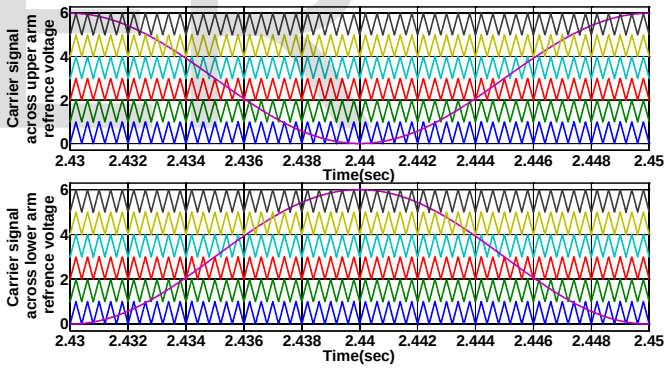

Figure 7. The reference signals for both the upper and lower arms across the carrier signal.

A sinusoidal waveform in the output can therefore be achieved by varying the number of submodules in the upper and lower arms in a sinusoidal manner. Since the voltage of each arm is not continuous but varies based on the switching of the submodules, the selection of the submodules and the PWM method applied to the converter affect its operation and output waveforms. The two arms that comprise the phase leg of the converter can be modulated either simultaneously or independent of each other. The number of submodules to insert or bypass was found by comparing the voltage reference with the carrier waves. The selection of submodules which is the next step can be done based on the capacitor voltage measurements delivered from the submodules. When the multivalve current direction is known, one can predict whether the capacitor will charge or discharge when inserted. This infor-

mation is used to insert or bypass the submodules closest to the range limits, which keeps the capacitors' voltages balanced in this way. A positive current will charge the inserted capacitors, while a negative current will discharge the capacitors. This leads to the next step, which is called submodule selection.

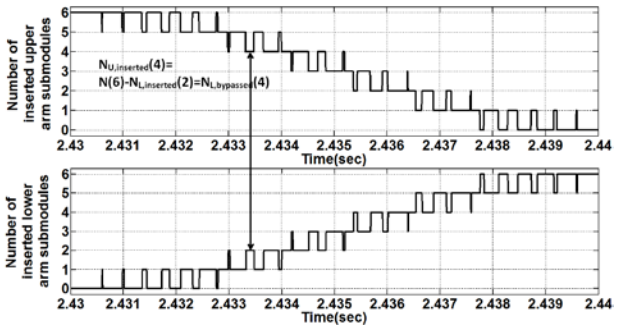

Figure 8. Number of inserted submodules for upper and lower arms.

3.4 Submodules selection

To maintain the individual voltage of each submodule around its reference voltage takes an active balancing method. The voltage of each individual submodule together with the arm current needs to be measured and available in the voltage-balancing algorithm. The voltage-balancing algorithm selects the submodules in each of the arms of the converter based on the relative voltage values of all the arm submodules and direction of the arm current. Ascending or descending capacitor voltages are required to be used for balancing algorithm. The next submodule that switches in the arm is selected based on the direction of the current and the sorted voltages so that

If the arm current is positive ($i_{arm} > 0$) and the modulation process method requires the subtraction of one submodule in the arm, the balancing algorithm will select the submodule with the highest voltage that is connected to the arm to be bypassed and removed from the arm.

If the arm current is negative ($i_{arm} > 0$) and the modulation process method requires the addition of one submodule in the arm, the balancing algorithm will select the submodule with the highest voltage that is not connected to the arm to be inserted to the arm.

If the arm current is negative ($i_{arm} < 0$) and the modulation process method requires the subtraction of one submodule in the arm, the balancing algorithm will select the submodule with the lowest voltage that is connected to the arm to be bypassed and removed from the arm.

The capacitor voltage of the submodule will not change when the submodule is not connected to the arm of the converter; it will remain at the level it was before it was removed from the arm of converter. The voltage balancing algorithm uses the data coming from the modulation process, upper and lower arms currents, and upper and lower arms sorting voltages. Figure 3 shows the proposed PWM algorithm sorting both arms voltages. The main aim of the selection process is to maintain the voltages of the capacitors close to the reference values. This is accomplished during the whole cycle of the waveform and the capacitors' actual voltages drift from their reference value within this cycle due to the load current coming from upper and lower arms currents. Moreover, the algorithm considers the actual values for capacitor voltages coming from voltages measurements after sorting them in

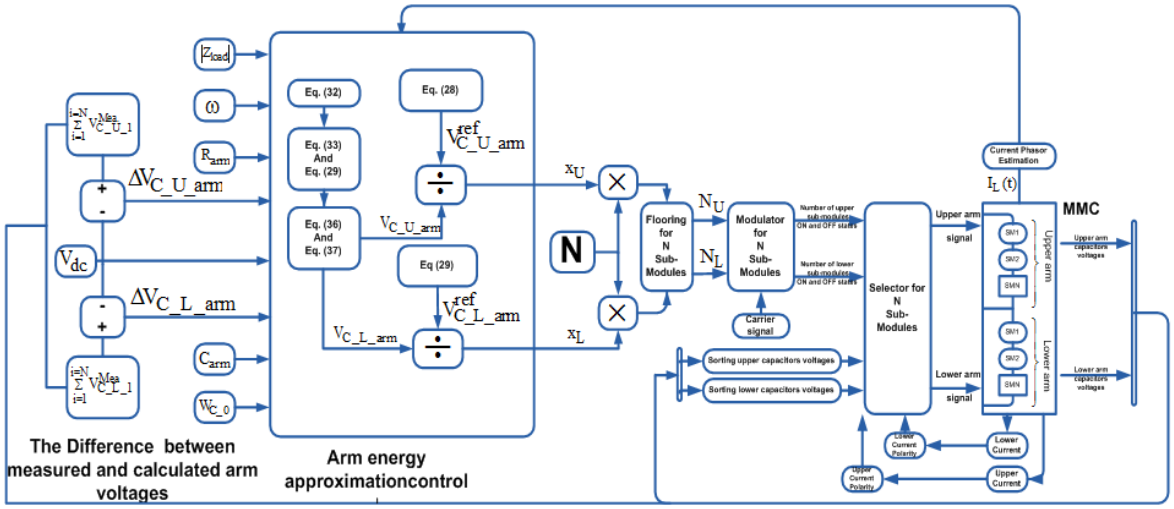

Figure 9. Proposed PWM algorithm with sorting voltage for MMC.

When the arm current is positive ($i_{arm} > 0$) and the modulation process method requires the addition of one submodule in the arm, the balancing algorithm will select the submodule with the lowest voltage that is not connected to be inserted into the arm.

the selection of the submodules, but their relative voltage relates to the remaining submodules in the arm. In some cases, the submodule selected to be inserted into the arm of the converter according to the logic of the algorithm will further deviate from the reference voltage. The balancing of the submo-

dule is not an instantaneous process and balancing around the reference occurs over the fundamental period.

4. SIMULATION RESULTS

A number of simulations in MATLAB/Simulink have been verified through the operation of MMC under the proposed control. The results for the 481-level in the output voltage waveform have been considered for the N + 1 approach towards MMC using the proposed algorithm. The case of the N + 1 approach and a converter with 480 submodules per arm is considered to derive a waveform with an odd number of levels. Time simulations were conducted on an MMC model to evaluate the proposed algorithm. The ratings of the simulated converter are again given in Table III.

TABLE III
SIMULATION PARAMETERS FOR THE N+1 MODULATION

Parameters	N + 1 approach	Parameters	N + 1 approach
DC bus	2,200 KV	L_{arm}	0.485 H
R_{load}	130 Ω	Submodule voltage	5.5 KV
L_{load}	130 mH	R_{arm}	3 Ω
Module capacitance C	28.4 mF	Target capacitor voltage ripple	%5
Number of submodules per arm	480	Number of output levels	481
Load factor		0.95	

The main idea is to prove that this proposed algorithm is quite efficient, even though it is not based on any internal state measurements. Figures 10 to 13 show the simulation results for the proposed algorithm. In Figure 10, the output voltage and current is purely sinusoidal.

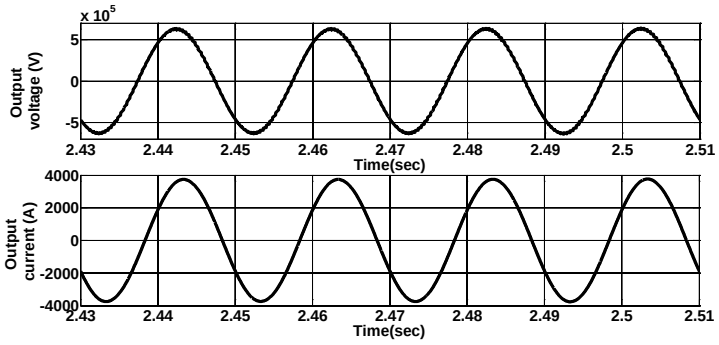

Figure 10. AC output phase voltage and current for MMC at the 481 level by using the proposed control.

However, the arm currents, which are shown in Figure 11, seem to contain very small second harmonic components.

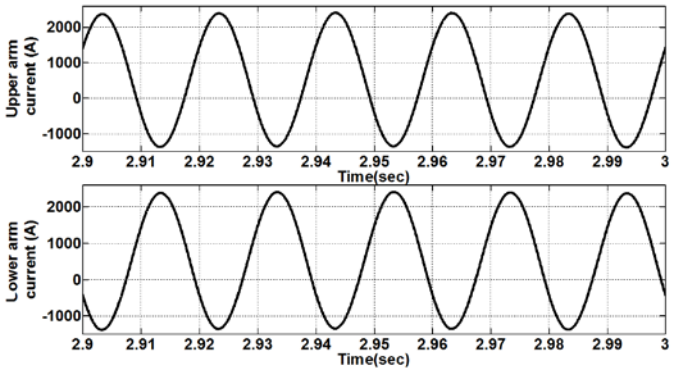

Figure 11. Upper and lower arms' currents for MMC at the 481 level by using the proposed control.

Figure 12 shows the intermediate capacitors' voltages for the both upper and lower arms. The target ripple for each capacitor voltage (5.4%) had almost been achieved, at less than 6.2%. In addition, the circulating current I_{cir}, periodic with 10 ms cycle, had a small amplitude of about 60 A from peak to peak, with ripple less than 7.2%, as shown in Figure 13.

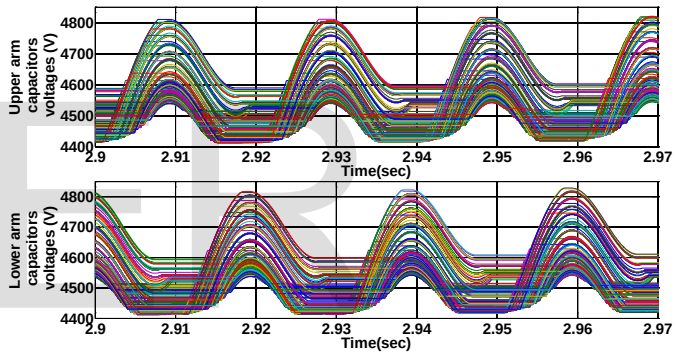

Figure 12. Upper and lower arms' intermediate capacitor voltages for MMC at the 481 level by using the proposed control.

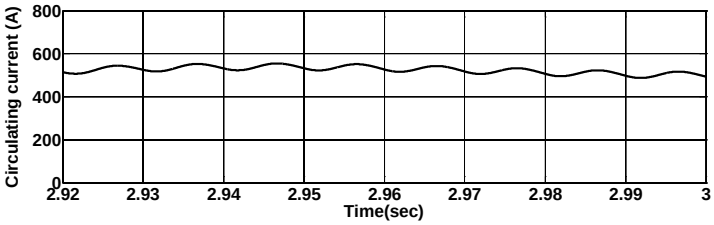

Figure 13. Circulating current for MMC at the 481 level using the proposed control.

The FFT analysis for the arm currents and the output voltage of one phase leg were recorded. The arms' current THD factor reached 1.47%. The output voltage THD factor reached 0.63%. Finally, the output current THD factor reached 0.11%. All of the above indicate that the agreement between the use of the proposed algorithm for MMC and the required THD at the AC side to avoid using filters is rather satisfactory.

5. EXPERIMENTAL RESULTS

The proposed control for MMC was also verified on a phase-

leg experimental prototype with two submodules per arm. The specifications of the laboratory prototype are given in Table IV. The modulation and voltage sorting and balancing algorithms were implemented using the DSP F2812 board. The final form of a prototype MMC board is equipped with eight switches on a heat sink, as depicted. Each submodule needs a blocking ability of about 200 to 275 volts. The proposed control for MMC was tested first, as a final MMC control validation approach. The results, given below, correspond to a single-phase operation with 4 kHz switching frequency. Figure 14 shows the output voltage of the 3-level modulation concept and output phase current. The voltage inside each level varies, since the capacitor voltages are not constant.

TABLE IV
MMC laboratory prototype specifications

Parameters	Values
DC voltage	500 V
R_{load}	20 Ω
L_{load}	2.2 mH
Submodules capacitance	2.2 mF
Arm inductance	3.5 mH
Arm resistance	0.1 Ohm
Number of submodules per arm	2
Submodules voltage	250 V
Number of output level	3
Reference frequency	50Hz
Carrier frequency	3KHz

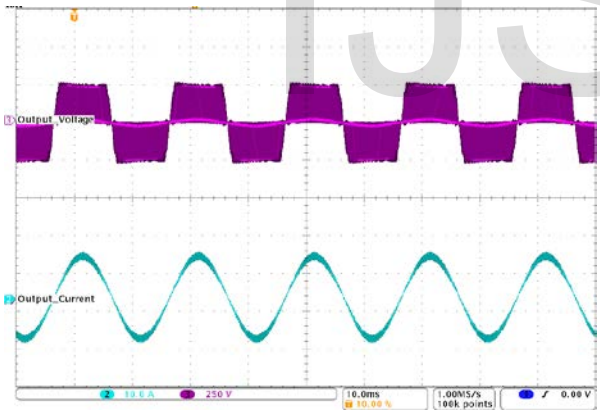

Figure 14. Experimental results: Three-level phase-voltage and load current.

Figure 15 shows the results of upper and lower arms' currents (first and second from top to bottom), as described in (5) (which is given at the bottom of Figure 15 1 − 2), giving the output current (fourth, from top to bottom) and the measured output current waveform (third, from top to bottom). The upper arm current generates the positive half cycle for the AC output current, and the lower arm current generates its negative half cycle.

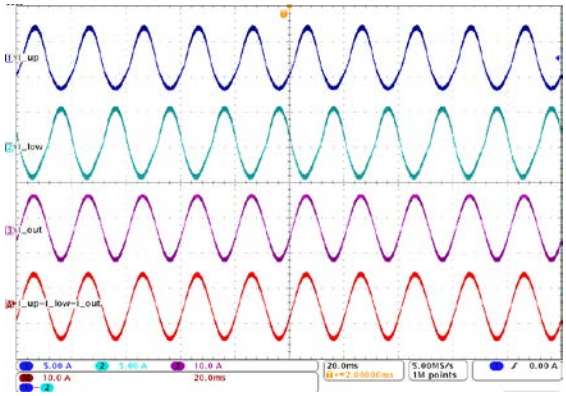

Figure 15. Experimental results, from top to bottom: Upper arm current, lower arm current, measured output current and calculated output current of MMC.

Figure 16 shows the results of the upper (at top) and lower (at bottom) arms' voltages, as described in (9), giving the output voltage (middle). Unlike the output current waveform, the upper arm voltage generates the negative half cycle for AC output voltage, while the lower arm voltage generates its negative half cycle.

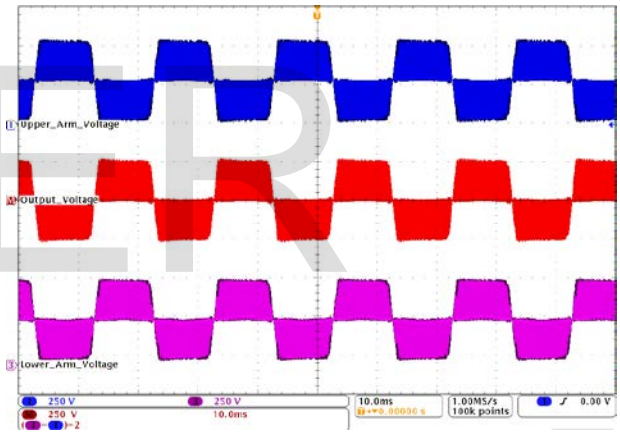

Figure 16. Experimental results: Upper arm voltage (top), lower arm voltage (bottom) and output voltage (middle) of the MMC

The waveform circulating current, Icir, of a 10 ms period, shown in Figure 17, is as expected.

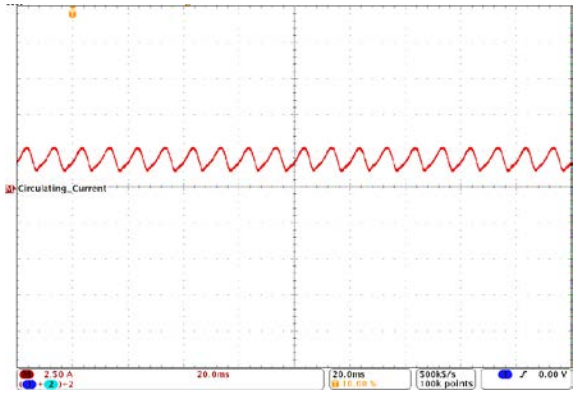

Figure 17. Experimental results: Circulating current through the circuit of the MMC

6. CONCLUSION

In this paper, the closed–loop, needless PID controller based on the difference between the measured voltage and calculated voltage of each arm of the MMC was derived and presented, describing the main idea of MMC acting in a single phase. A new control for MMC is introduced with this closed-loop, needless PID controller, for use with a wide range of number of submodules that can be used for high and extra-rate power applications. Insertion indices equations were generated that utilized the difference between the measured and calculated voltages of each arm of the MMC, which were considered the starting point for the proposed control, for which the number of submodules per arm (N) was derived. The modulation process was also explained in detail, in order to show that this method can be used with a wide range of submodules to achieve a large number of levels for the output voltage that reduce the THD. The proposed PWM control comes to fulfill the requirements of UHVDC bus voltage in this paper with many contributions. Since there will be demand for UHVDC in the next years (2200 KV and more) The paper proposes MMC topology with more submodules per arm to achieve large scale of output voltage levels based on simple algorithm control. Also, Since the number of submodules is hundreds in UHVDC, sinusoidal AC voltage waveforms will be achieved and THD will be limited to less than one to avoid using AC filters. The proposed method works with low switching frequency for UHVDC systems, which will decrease converter losses. Moreover, for MMC itself the proposed method offers simple numerical algorithm for MMC topology that can be used with large or small number of submodules per arm either experimentally or by simulation. Selection process for inserting or bypassing submodules guarantees capacitors voltages around the reference voltage (Vdc/N) with voltage ripple less than 7% even for large number of submodules per arm. More converter stability can be achieved by equal sharing of currents from both arms to the load. Overall, the proposed PWM allows MMC to be used with large scale of power transmission either HVDC systems or large scale of solar energy and also can be used for large motors control. The theoretical analysis was verified through extended simulation results at the 481 submodule–level, as well as experimentally on a laboratory prototype phase-leg of the MMC with four submodules, based on arm energy approximation control.

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